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EXAMINER

DIVECHA, KAMAL B

ART UNIT	PAPER NUMBER
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2151

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

10/000,456

Applicant(s)

KAGAN ET AL.

Examiner

KAMAL B. DIVECHA

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-59 is/are pending in the application.
- 4a) Of the above claim(s) 20-30 and 50-59 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 and 31-49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>20020204</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1-19 and 31-49 are pending in this application and are presented for examination.

Applicant, in response to restriction/election filed on August 29, 2005, has elected Group I (claims 1-19 and 31-49) without traverse.

Priority

Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged.

Information Disclosure Statement

The information disclosure statement (IDS) submitted is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code (page 1). Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

The incorporation of essential material in the specification by reference to an unpublished U.S. application, foreign application or patent, or to a publication is improper. Applicant is required to amend the disclosure (page 17-18) to include the material incorporated by reference, if the material is relied upon to overcome any objection, rejection, or other requirement imposed by the Office. The amendment must be accompanied by a statement executed by the applicant, or a practitioner representing the applicant, stating that the material being inserted is the material

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previously incorporated by reference and that the amendment contains no new matter. 37 CFR 1.57(f).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 5, 6, 9, 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation “the queues”, “the instances”, “the schedule queues” in the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 6 recites the limitation “the instances”, “the queues”, and “the execution engines”. There is insufficient antecedent basis for this limitation in the claim.

Claim 9 recites the limitation “the queues” in the claim. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 16, the phrase "such packets" renders the claim indefinite because it is unclear whether the packets are outgoing response packets, incoming read request packets, outgoing or incoming write packets.

Claim 17 recites the limitation “the plurality of the instances” in the claim. There is insufficient antecedent basis for this limitation in the claim.

Please Note the listing above is not the exhaustive listings of all the 35 USC 112, 2nd paragraph rejections. The listing above is provided as an example and it is up to the applicant to fix the rest.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4-5, 7, 9, 10, 12, 14-19, 31, 34-35, 37-38, 40, 42 and 44-49 are rejected under 35 U.S.C. 102(e) as being anticipated by Pettey et al. (U. S. Patent No. 6,594,712 B1).

As per claim 1, Pettey discloses a network interface adapter, comprising: a host interface for coupling to a host processor (fig. 2 item #206, fig. 18b item #308); an outgoing packet generator for delivery to a remote responder responsive to a request submitted by the host processor via the host interface col. 7 L65 to col. 8 L7, col. 14 L20-39, fig. 3 item #306); a network output port, coupled to receive the request packet from the output packet generator, so as to transmit the outgoing request packet over a network to the remote responder (col. 9 L1-5, fig. 3 item #308); a network input port, for coupling to the network so as to receive an incoming response packet from the remote responder, in response to the outgoing request packet sent thereto, and further to receive an incoming request packet sent by a remote requester (fig. 3 item #308 and fig. 2 item #204); an incoming packet processor, coupled to the network input port so as to receive and process both the incoming response packet and the incoming request packet, and further coupled to cause the outgoing packet generator, responsive to the incoming request packet, to generate in addition to the outgoing request packet, an outgoing response packet for

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transmission via the network output port to the remote requester (col. 10 L4-9, col. 14 L40-54 and fig. 3 item #306).

As per claim 4, Pettey discloses an interface adapter wherein the outgoing packet generator comprises a plurality of schedule queues (fig. 7a block #108), and is adapted to generate the outgoing request packet (fig. 16) and the outgoing response packet responsive to respective entries placed in the queues (fig. 18a item #1808, 1822, fig. 22a item #2224, 2226 and fig. 15).

As per claim 5, Pettey discloses an interface adapter wherein the network input and output ports are adapted to receive and send the incoming and outgoing packets, respectively, over a plurality of transport service instances, and wherein the outgoing request packet and the outgoing response packet are associated with respective instances among the plurality of transport service instances (fig. 7a item #108), and wherein the outgoing packet generator is adapted to assign the transport service instances to the queues based on service parameters of the instances, and to place the entries in the schedule queues corresponding to the transport service instances with which the incoming and outgoing packets are associated (col. 8 L2-26, col. 11 L1-36 and col. 14 L10-54 and col. 17 L20-40).

As per claim 7, Pettey discloses an adapter wherein the transport service instances comprise queue pairs (fig. 7a-7b: shows plurality of queues including queue pairs).

As per claim 9, Pettey discloses an adapter wherein the incoming request packet comprises a write request packet carried over the network on a reliable transport service, and wherein responsive to the incoming write request packet, the incoming packet processor is

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adapted to add an entry to the entries placed in the queues, such that responsive to the entry, the outgoing packet generator generates an acknowledgement packet (col. 19 L55 to col. 20 L33).

As per claim 10, Pettey disclose an adapter wherein the incoming request packet comprises an incoming read request packet, and wherein responsive to the incoming read request packet, the incoming packet processor is adapted to prepare a read response work item in a memory location, and wherein the outgoing packet generator is coupled to read the response work item from the memory location and, responsive thereto, to generate a read response packet (fig. 15: describes an incoming read request packet, and col. 13 L58 to col. 14 L9, L40-65 and col. 15 L65 to col. 16 L6).

As per claim 12, Pettey discloses an adapter wherein the incoming packet processor is configured so that when it receives an incoming write request packet containing write data to be written to a system memory accessible via the host interface before receiving the incoming read request packet, it prevents execution of the read response work item until the write data have been written to the system memory (col. 21 L12 to col. 22 L6).

As per claim 14, Pettey discloses an adapter wherein the outgoing packet generator is adapted, upon generating the outgoing request packet, to notify the incoming packet processor to await the incoming response packet so as to write a completion message to the host interface when the awaited packet is received (col. 20 L17-32).

As per claim 15, Pettey discloses an adapter wherein the incoming request packet comprises an incoming read request packet specifying data to be read from a system memory accessible via the host interface, and wherein the incoming packet processor is adapted to write a response descriptor to a memory location indicating the data to be read from the system memory

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responsive to the read request packet (fig. 18a item #1822), and wherein the outgoing packet processor is adapted to read the response descriptor from the memory location and, responsive thereto, to read the indicated data and to generate the outgoing response packet containing the indicated data (fig. 18a item #1832; col. 15 L5 to col. 16 L6).

As per claim 16, Pettey discloses an adapter wherein the incoming read request packet is one of a plurality of incoming read request packets, and wherein the incoming packet processor is adapted to write the response descriptor to the memory location as part of a list of such descriptors, responsive to which the outgoing packet processor is adapted to generate the outgoing response packet as part of a sequence of such packets (fig. 19a, fig. 20 and fig. 9; col. 23 L20 to col. 24 L27; col. 11 L18-37).

As per claim 17, Pettey discloses an adapter wherein the network input and output ports are adapted to receive and send the incoming and outgoing packets, respectively, over a plurality of transport service instances, and wherein the incoming packet processor is adapted to prepare the list of the response descriptors for each of the instances as a part of a response database held for the plurality of the instances in common (fig. 3 item #308, fig. 19b item #508, and fig. 23).

As per claim 18, Pettey discloses an adapter wherein the transport service instances comprise queue pairs (fig 7a item #712).

As per claim 19, Pettey discloses an adapter wherein the request comprises a write request, which is submitted by the host processor by generating a request descriptor indicating further data to be read from the system memory for inclusion in the outgoing packet (fig. 10), and wherein the output packet generator is adapted to read the request descriptor and, responsive

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thereto, to generate the outgoing request packet as a write request packet containing the indicated further data (fig. 18a item #1832; col. 12 L58 to col. 13 L18, col. 15 L17-31 and fig. 16).

As per claims 31, 34-35, 37-38, 40, 42, 44-49, they do not teach or further define over the limitations in claims 1, 4-5, 7, 9, 10, 12 and 14-19. Therefore claims 31, 34-35, 37-38, 40, 42, 44-49 are rejected for the same reasons as set forth in claims 1, 4-5, 7, 9, 10, 12 and 14-19.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 8 and 39 are rejected under 35 U.S.C. 103(a) as being obvious over Pettey et al. (U. S. Patent No. 6,594,712 B1) in view of Collins et al. (hereinafter Collins, Pub. No.: US 2002/0144001 A1).

As per claim 8, Pettey discloses an adapter wherein the outgoing packet generator comprises one or more control registers to which the host processor and incoming packet

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processor write in order to place the entries in the queues (col. 17 L20-56), however Pettey does not explicitly disclose the one or more register to be a doorbell registers.

Collins, from the same field of endeavor explicitly discloses a channel adapter comprising one or more doorbell registers (fig. 9, page 8 block #[0075], [0079]). Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view of Collins, in order to replace the one or more control registers with the doorbell registers, since Collins teaches and discloses the usage of doorbell registers. One of ordinary skilled in the art would have been motivated because doorbell registers allows software the capability to enable automatic event generation, and making doorbell registers memory mapped allows applications the ability to write those registers thereby controlling event generation (Collins, page 8 block #[0075] and [0079]).

As per claim 39, it does not teach or further define over the limitations in claim 8. Therefore claim 39 is rejected for the same reasons as set forth in claim 39.

4. Claims 11 and 41 are rejected under 35 U.S.C. 103(a) as being obvious over Pettey et al. (U. S. Patent No. 6,594,712 B1).

As per claim 11, Pettey discloses the process of receiving a read request (fig. 15 item #1000); the process of receiving a write request (fig. 16 item #1000); and the process of conveying or sending the write data to the host interface (fig. 15 item #1100), however Pettey does not disclose the process of receiving an incoming write request packet containing write data to be written to a system memory accessible via the host interface after receiving the incoming read request packet, and the process of conveying the write data to the host interface without waiting for execution of the read response work item. But it would have been obvious to a person

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of ordinary skilled in the art at the time the invention was made to modify Pettey (i.e. modify Pettey's figure 15 and 16 so that the incoming packet processor of the adapter (see the rejected claim 1) is configured so that the write request work queue entry is executed first with respect to read response work queue entry) in order to convey the write data to the host interface without waiting for execution of the read response work item, since Pettey teaches receiving incoming write request, receiving incoming read request packet, executing both of the requests, and conveying the write data to the host interface. One of ordinary skilled in the art would have been motivated because it would have improved the efficiency and enhanced the performance of the interface adapter.

As per claim 41, it does not teach or further define over the limitation in claim 11.

Therefore claim 41 is rejected for the same reasons as set forth in claim 11.

5. Claims 2-3, 6, 13, 32-33, 36 and 43 are rejected under 35 U.S.C. 103(a) as being obvious over Pettey et al. (U. S. Patent No. 6,594,712 B1) in view of Gasbarro et al. (hereinafter Gasbarro, U. S. Patent No. 6,948,004 B2).

As per claim 2, Pettey discloses an adapter wherein the outgoing request packet comprises an outgoing write request packet containing write data taken from a system memory accessible via the host interface (fig. 18a: describes the process of RDMA WRITE operation; fig. 16 shows the I/O WRITE operation), wherein the outgoing response packet comprises an outgoing read response packet containing read data taken from the system memory in response to the incoming request packet (fig. 18a and fig. 16) and a scatter/gather list created by CPU (fig. 9), however Pettey does not explicitly disclose the process of gathering both the write data and the read data from the system memory for inclusion in the respective outgoing packets.

Gasbarro, from the same field of endeavor, explicitly discloses an interface adapter (fig. 7) comprising a gather engine providing a gather list describing virtual addresses to fetch outgoing data from local system memory (col. 8 L10-34). Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view of Gasbarro, in order to gather both the write data and the read data from the system memory for inclusion in the respective outgoing packets, since Gasbarro teaches the process of gathering outgoing data from the system memory.

One of ordinary skilled in the art would have been motivated because it would have enabled the process of fetching outgoing data from system memory (Gasbarro, col. 8 L28-34).

As per claim 3, Pettey discloses an adapter wherein to submit the request, the host processor writes a request descriptor indicative of the write data to a first memory location, and wherein to cause the outgoing packet generator to generate the outgoing response packet, the incoming packet processor writes a response descriptor indicative of the read data to a second memory location (this approach is known as double buffering, col. 11 L18 to col. 12 L45 and fig. 7b) and wherein the WQE includes SGL local address field for specifying the physical address in local memory of a scatter/gather list, however Pettey does not disclose a process adapted to read information from the descriptors and to gather the read data and the write data responsive thereto. Gasbarro discloses a scatter/gather engine adapted to read information from the indicators or descriptors and to gather or fetch the read data and the write data (col. 8 L28-41). Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view of Gasbarro, in order to read information from the descriptors and to gather or fetch the write data and the read data from the system memory, since

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Gasbarro teaches the process of gathering outgoing data from the system memory. One of ordinary skilled in the art would have been motivated because of the same reasons as set forth in claim 2.

As per claim 6, Pettey discloses an adapter wherein the outgoing packet generator comprises one or more execution engines, which are adapted to generate the outgoing request packet and the outgoing response packet responsive to a list of work items respectively associated with each of the transport service instances (col. 1 L54 to col. 2 L21, col. 7 L65 to col. 8 L7, col. 11 L18-53), however Pettey does not disclose a scheduler, which is coupled to select the entries from the queues and to assign the instances to the execution engines for execution of the work items responsive to the service parameters. Gasbarro discloses an adapter comprising a scheduler for scheduling the next virtual interface to the context manager and supporting priority of traffic for data packets associated with send Queue and Receive Queue of the work queue pair (col. 15 L50-58). Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view Gasbarro, in order to include a scheduler for selecting the entries from the queues and to assign the instances to the execution engines for execution of the work items responsive to the service parameters. One of ordinary skilled in the art would have been motivated because a scheduler would have supported the priority of traffic for data packets associated with Send queue and Receive queue of the work queue pair (Gasbarro, col. 15 L50-55).

As per claim 13, Pettey discloses the adapter wherein the incoming response packet comprises an incoming read response packet sent by the remote responder in response to the outgoing request packet, the incoming read response packet containing read data to be written to

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a system memory accessible via the host interface, and wherein the incoming request packet comprises an incoming write request packet containing write data to be written to the system memory (fig. 16), however Pettey does not disclose a scatter engine, which is coupled to scatter both the write data and the read data from the respective incoming packets to the system memory. Gasbarro, from the same field of endeavor, discloses an adapter comprising a scatter engine providing a scatter list describing the virtual addresses to place incoming data in local system memory (col. 8 L10-40). Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view of Gasbarro, in order to scatter both the write data and the read data from the respective incoming packets to the system memory, since Gasbarro teaches the process of placing the incoming data to the systems memory. One of ordinary skilled in the art would have been motivated because scatter engine would have describe exactly where to store incoming data within local system memory (col. 8 L35-40).

As per claims 32-33, 36 and 43, they do not teach or further define over the limitations in claims 2-3, 6 and 13. Therefore claims 32-33, 36 and 43 are rejected for the same reasons as set forth in claims 2-3, 6 and 13.

Additional References

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. Beukema et al., U. S. Patent No. 6,578,122 B2.
- b. Avery, U. S. Patent No. 6,611,883 B1.

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- c. Thomas et al., U. S. Patent No. 5,922,046.
- d. Coffman et al., U. S. Patent No. 6,718,370 B1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAMAL B. DIVECHA whose telephone number is 571-272-5863. The examiner can normally be reached on Flex schedule 8 hr days (10.00am-6.30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarni Maung can be reached on 571-272-3939. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


October 5, 2005.


ZARNI MAUNG
SUPERVISORY PATENT EXAMINER